

AT  
Conced  
457  
cont'd

3 p-channel typ MIS transistor and an n-channel type MIS  
4 transistor to which a substrate bias is applied in a reverse  
5 direction by the potential of said well region, and said  
6 second logic gate includes a p-channel type MIS transistor and  
7 an n-channel type MIS transistor to which a substrate bias is  
8 applied in a forward direction by a potential of said well  
9 region.

10. (Amended) A semiconductor integrated circuit  
according to claim 6, wherein said first logic gate includes a  
p-channel type MIS transistor to which a substrate bias is  
applied in a reverse direction by a potential of said well  
region, and said second logic gate includes a p-channel type  
MIS transistor to which a substrate bias is applied in a  
forward direction by a potential in said well region.

11. (Amended) A semiconductor integrated circuit  
according to claim 6, wherein said first logic gate includes a  
p-channel type MIS transistor and an n-channel type MIS  
transistor to which a substrate bias is applied in a reverse  
direction by a potential in said well region.

---

Please add the following new claims:

---

A<sub>2</sub>

39. (New) A semiconductor integrated circuit according  
to claim 7, wherein said first logic gate includes an MIS  
transistor to which a substrate bias is appli d in a reverse

A2  
Cont.

4 direction by a potential in said well region, and said second  
5 logic gate includes an MIS transistor to which a substrate  
6 bias is applied in a forward direction by a potential in said  
7 well region.

03855603 051604

1 40. (New) A semiconductor integrated circuit according  
2 to claim 7, wherein said first logic gate includes a p-channel  
3 type MIS transistor and an n-channel type MIS transistor to  
4 which a substrate bias is applied in a reverse direction by  
5 the potential of said well region, and said second logic gate  
6 includes a p-channel type MIS transistor and an n-channel type  
7 MIS transistor to which a substrate bias is applied in a  
8 forward direction by a potential of said well region.

1 41. (New) A semiconductor integrated circuit according  
2 to claim 7, wherein said first logic gate includes a p-channel  
3 type MIS transistor to which a substrate bias is applied in a  
4 reverse direction by a potential of said well region, and said  
5 second logic gate includes a p-channel type MIS transistor to  
6 which a substrate bias is applied in a forward direction by a  
7 potential in said well region.

1 42. (New) A semiconductor integrated circuit according  
2 to claim 7, wherein said first logic gate includes a p-channel  
3 type MIS transistor and an n-channel type MIS transistor to